Decision Feedback Equalizers Using the Back-Gate Feedback Technique

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***Abstract*—A merged adder/D-type flip-flop (DFF) is presented by using the back-gate feedback technique. By using this merged adder/DFF, a slicerless one-tap decision feedback equalizer (DFE) and a cascaded DFE are fabricated in 65-nm CMOS technology. For a cable loss of 12 dB and a 30-Gb/s pseudorandom bit sequence (PRBS) of $2^7 - 1$, the measured bit error rate of the slicerless one-tap DFE is below 10^{-11}. Its power dissipation is 27 mW from a 1-V supply. For a cable loss of 12 dB and a 30-Gb/s PRBS of $2^{15} - 1$, the measured bit error rate of the cascaded DFE is below 10^{-12}. This cascaded DFE consumes 55 mW from a 1-V supply.**

***Index Terms*—Back gate, channel loss, decision feedback equalizer (DFE), feedback, intersymbol interference (ISI).**

I. Introduction

DECISION feedback equalizers (DFEs) [1]–[8] are widely used in various wireline communications to compensate the intersymbol interference (ISI) caused by channel loss. In multigigabits-per-second applications, there are several design challenges for DFEs, such as operation speed, jitter, area, and power consumption. To recover the data suffered from the severe channel loss, multiple-tap DFEs [1]–[4] are usually adopted to have better eye opening and a lower jitter.

Fig. 1 shows a conventional multiple-tap DFE, which is composed of an adder, a slicer, and D-type flip-flops (DFFs). In this DFE, the previous bits must be multiplied with tap weightings and feed back to an adder. The multiple-tap DFE results in a large parasitic capacitance value for the adder to degrade the bandwidth [2]. To compensate the ISI caused by the previous bits, this adder has to complete the operation within 1-b time. It results in a critical path in a multiple-tap DFE and limits the operation speed, as shown in Fig. 1. Compared with a multiple-tap DFE, a one-tap DFE may be suitable for high-speed applications, but the capability to compensate the channel loss is limited. Moreover, the output common-mode voltage and swing of an adder are varied according to the tap weighting. Thus, a slicer is needed, which increases the capacitance loading for an adder, and additional power is also needed.

To increase the operation speed, a 40-Gb/s one-tap DFE with a back-gate feedback adder is presented [6]. The back-gate feedback adder not only isolates the parasitic capacitance

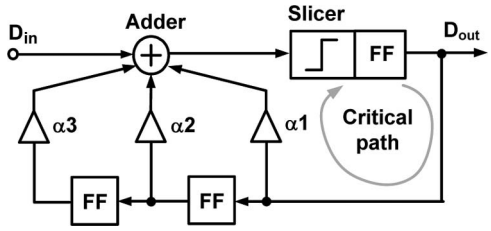

Fig. 1. Conventional multiple-tap DFE.

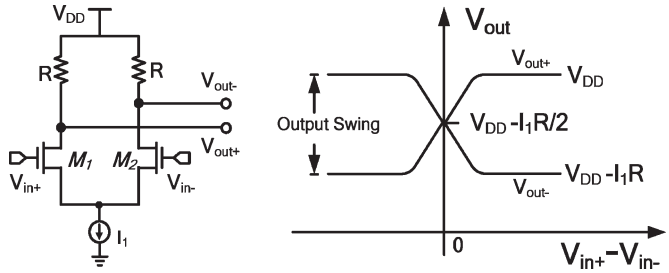

Fig. 2. Differential pair and its input–output transfer curve.

introduced by the feedback tap but also reduces the threshold voltages of the MOS transistors of the input stage. Hence, the operation speed of a DFE is improved. Although the back-gate feedback DFE achieves a data rate of 40 Gb/s, many passive inductors are adopted and it results in a large active area.

In this brief, to enhance the operation speed without passive inductors, a slicerless one-tap DFE using the proposed merged adder/DFF is presented. To improve the jitter performance and enlarge the vertical eye opening without speed penalty, a cascaded DFE is also presented. This brief is organized as follows. Section II describes the merged adder/DFF, a one-tap DFE, and a cascaded DFE. Section III shows the experimental results. The conclusions are given in Section IV.

II. Circuit Description

A. Conventional Adder

Fig. 2 shows a differential pair with tail current I_1 and two resistors R. When input signal $V_{\text{in}+}$ is much lower than $V_{\text{in}-}$, M_1 is off and M_2 is on, i.e., $V_{\text{out}-} = V_{DD} - I_1R$ and $V_{\text{out}+} = V_{DD}$. On the other hand, when $V_{\text{in}+}$ is much higher than $V_{\text{in}-}$, M_1 is on and M_2 is off, i.e., $V_{\text{out}+} = V_{DD} - I_1R$ and $V_{\text{out}-} = V_{DD}$. Note that the maximum and minimum output voltages of this differential pair are V_{DD} and $V_{DD} - I_1R$, respectively. In addition, its output common-mode voltage is equal to $V_{DD} - I_1R/2$.

Fig. 3(a) shows a one-tap DFE using a conventional adder, where the main tap has tail current I_1, and the feedback tap has

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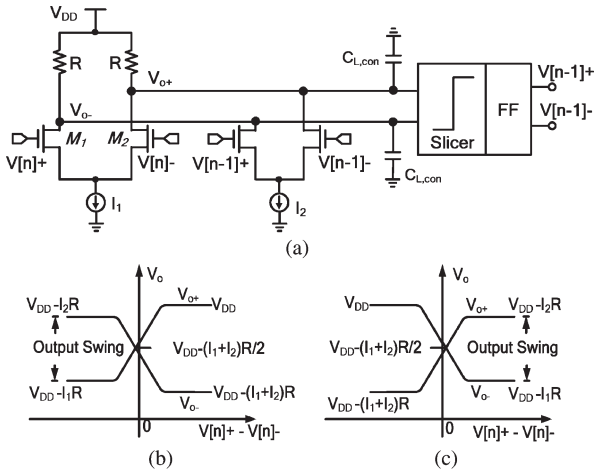

Fig. 3. (a) One-tap DFE and the input–output transfer curves while (b) $V[n-1]+$ is high and $V[n-1]-$ is low, and (c) $V[n-1]+$ is low and $V[n-1]-$ is high.

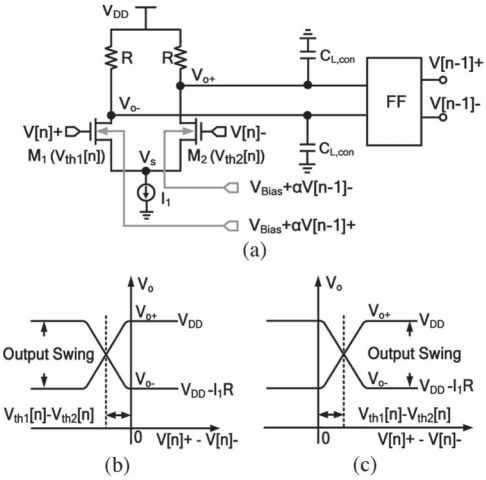

Fig. 4. (a) Back-gate feedback adder [6] in a one-tap DFE and its input–output characteristics while (b) $V[n-1]+$ is high and $V[n-1]-$ is low, and (c) $V[n-1]+$ is low and $V[n-1]-$ is high.

tail current I_2. In general, I_2 is smaller than I_1. In Fig. 3(a), this adder is realized by a differential pair in Fig. 2. The present and previous bits are $V[n]$ and $V[n-1]$, respectively, and n is an index. Assume that $V[n-1]+$ is high and $V[n-1]-$ is low, the input–output transfer curve of this adder is shown in Fig. 3(b). The minimum output swing of this adder is from $V_{DD}-I_2R$ to $V_{DD}-I_1R$. Similarly, when $V[n-1]+$ is low and $V[n-1]-$ is high, the input–output transfer curve of this adder is shown in Fig. 3(c). The minimum output swing of this adder is from $V_{DD}-I_2R$ to $V_{DD}-I_1R$ too. Therefore, the minimum output swing and the common-mode voltage of this adder output are expressed as

$$(V_{DD}-I_2R)-(V_{DD}-I_1R)=(I_1-I_2)R \tag{1}$$

$$\frac{(V_{DD}-I_2R)+(V_{DD}-I_1R)}{2}=V_{DD}-\frac{(I_1+I_2)R}{2}. \tag{2}$$

In (1) and (2), the output common-mode voltage and the output swing of this adder depend upon tail current I_2. When tail current I_2 is adjusted to change the tap weighting, the output swing and common-mode voltage are varied too. To tolerate the nonconstant output swing and common-mode voltage, a slicer must be added between the adder and a DFF. However, to realize a high-speed and high-gain slicer, it should not only consume large power but it should also induce large parasitic capacitance [2]. To consider a one-tap DFE in Fig. 3(a), the parasitic capacitance values at the adder's output are given as

$$C_{L,\mathrm{con}}=C_{\mathrm{input\_stage}}+C_{\mathrm{feedback\_amp}}+C_{\mathrm{wire}}+C_{\mathrm{slicer}} \tag{3}$$

where $C_{\mathrm{input\_stage}}$, $C_{\mathrm{feedback\_amp}}$, C_{wire}, and C_{slicer} are contributed by the input stage, the feedback stage, interconnections, and the slicer itself, respectively. These parasitic capacitance values introduce a large RC time constant, which degrades the bandwidth of the adder and so does the DFE.

B. Adder Using the Back-Gate Feedback Technique

Fig. 4(a) shows an adder using the back-gate feedback technique in a one-tap DFE [6] and its input–output characteristics. $V_{\mathrm{th1}}[n]$ and $V_{\mathrm{th2}}[n]$ represent the threshold voltages of nMOS transistors M_1 and M_2, respectively. They are expressed as

$$V_{\mathrm{th1}}[n]=V_{\mathrm{th0}}+\gamma \cdot\left(\sqrt{|2\Phi_F+(V_S-V_{\mathrm{Bias}}-\alpha\cdot V[n-1]+)|}-\sqrt{|2\Phi_F|}\right) \tag{4}$$

$$V_{\mathrm{th2}}[n]=V_{\mathrm{th0}}+\gamma \cdot\left(\sqrt{|2\Phi_F+(V_S-V_{\mathrm{Bias}}-\alpha\cdot V[n-1]-)|}-\sqrt{|2\Phi_F|}\right) \tag{5}$$

where V_{th0} is the zero-biased threshold voltage, γ is the body effect coefficient, Φ_F is the surface potential, V_{Bias} is the output common-mode voltage of the level shifter, and α is the tap weighting. For this back-gate feedback adder, the present threshold voltages of M_1 and M_2 are dynamically changed by previous bit $V[n-1]$ and tap weighting α. Assuming that $V[n-1]+$ is high and $V[n-1]-$ is low, $V_{\mathrm{th1}}[n]$ is lower than $V_{\mathrm{th2}}[n]$. When $V[n-1]+$ is low and $V[n-1]-$ is high, $V_{\mathrm{th1}}[n]$ is higher than $V_{\mathrm{th2}}[n]$. The input–output characteristics are equivalently shifted from the origin to $V_{\mathrm{th1}}[n]-V_{\mathrm{th2}}[n]$ and $-(V_{\mathrm{th1}}[n]-V_{\mathrm{th2}}[n])$, as shown in Fig. 4(b) and (c), respectively. Since this adder does not execute at the current domain, its output swing and common-mode voltage are kept constant. They are expressed as

$$V_{DD}-(V_{DD}-I_1R)=I_1R \tag{6}$$

$$\frac{V_{DD}+(V_{DD}-I_1R)}{2}=V_{DD}-\frac{I_1R}{2}. \tag{7}$$

Therefore, a slicer is eliminated for a one-tap DFE using the back-gate feedback adder. This adder not only isolates the parasitic capacitance of the adder but also lowers the threshold voltage of the input stage to enhance the operation speed.

C. DFE Using a Merged Adder/DFF

Fig. 5 shows the proposed one-tap DFE, and it consists of a merged adder/DFF and a level shifter. Similar to an adder using

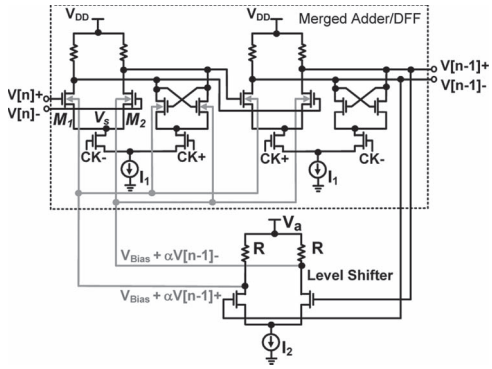

Fig. 5. One-tap DFE using the proposed merged adder/DFF.

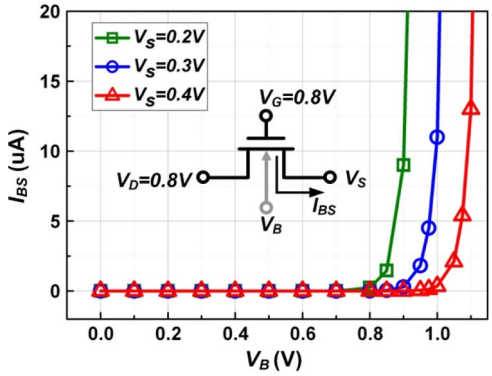

Fig. 6. Simulated bulk-to-source current I_{BS} versus bulk voltage V_B.

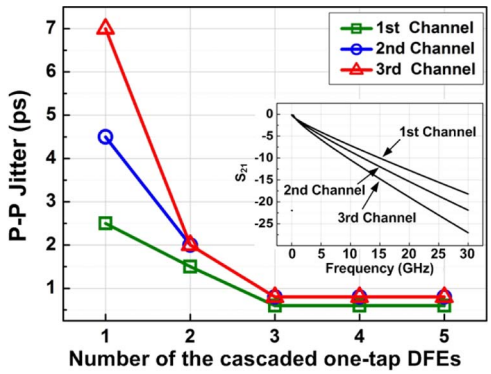

Fig. 7. Simulated peak-to-peak jitters versus the number of the cascaded one-tap DFEs under different channels.

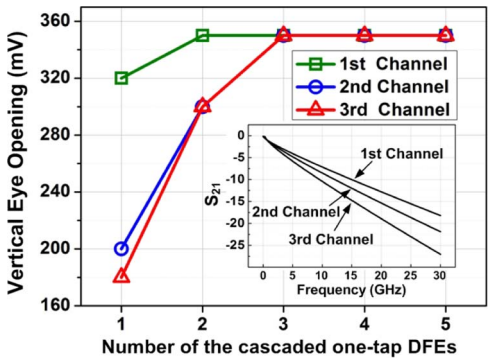

Fig. 8. Simulated vertical eye openings versus the number of the cascaded one-tap DFEs.

the back-gate feedback technique [6], the threshold voltages for the sampling and latching stages of the first latch and the sampling stage of the second latch are dynamically controlled by the level shifter in Fig. 5. The bulk of the latching stage on the second latch is grounded to keep a constant output. The area of each individual p-well surrounded by a deep n-well is $4.5 \times 5.5\ \mu\text{m}^2$. The extracted capacitance of each individual p-well is below 20 fF. By using the back-gate feedback technique, the threshold voltages and loading capacitance values are reduced to enhance the bandwidth. By using this proposed merged adder/DFF, the delay time of the critical path in a one-tap DFE is reduced to enhance the operation speed. Moreover, the power consumption of a one-tap DFE is also reduced. Thus, the proposed merged adder/DFF DFE achieves a high operation speed without passive inductors.

In Fig. 5, a level shifter is adopted to bias the bulk of the input transistors and adjust the tap weighting. The maximum and minimum output voltages of the level shifter are V_a and $V_a - I_2R$, respectively. One can find that V_{Bias} and α are $V_a - I_2R/2$ and $I_2R/2$, respectively. Therefore, the common-mode voltage V_{Bias} of the level shifter and tap weighting α are controlled by tail current I_2.

It is well known that one can raise the bulk voltage to reduce the threshold voltage for an nMOS transistor; however, forward biasing has to be avoided. It is interesting to know the limitation of the supply voltage V_a of this level shifter. Fig. 6 shows the simulation results of the bulk-to-source current I_{BS} versus the bulk voltage V_B and for an nMOS transistor in the 65-nm CMOS process. The gate and drain voltages for this nMOS transistor are set to the input and output common-mode levels of M_1 and M_2 in Fig. 5, respectively. The simulation results in Fig. 6 reveal that forward biasing occurs when the bulk-to-source voltage exceeds to 0.6 V. It means that, if the source voltage V_S of the differential pair in the back-gate feedback adder is 0.2 V, the maximum bulk voltage of M_1 and M_2 must be below 0.8 V to avoid forward biasing. Thus, the voltage V_a of this level shifter is 0.7 V in this brief. The threshold voltages of the differential pair M_1 and M_2 are changed for different tap weightings. Since the merged adder/DFF circuit has constant current sources, power consumption is slightly changed. Thus, the threshold voltages' sensitivity to the power consumption of the merged adder/DFF is low. For example, if the tail current I_2 of the level shifter is changed from 5 to 4 mA to adjust the tap weighting, the threshold voltage difference between the differential pair M_1 and M_2 becomes 62 mV. The power consumption values of the merged adder/DFF and the level shifter are decreased by 90 μW and 0.7 mW, respectively.

D. Cascaded DFE

To compensate the channel loss and suppress the ISI, multiple-tap DFEs are usually adopted. However, the multiple taps induce a large parasitic capacitance value and degrade the operation speed. To solve this problem, our idea is to cascade several one-tap DFEs to compensate the ISI.

The supply voltage of this one-tap DFE is 1 V, and the voltage V_a of this level shifter is 0.7 V. Tail currents I_1 and I_2 are 2.7 and 5 mA, respectively. For a 30-Gb/s pseudorandom bit sequence (PRBS) of $2^7 - 1$, Fig. 7 shows the simulated jitters of the retimed data versus the number of the cascaded one-tap

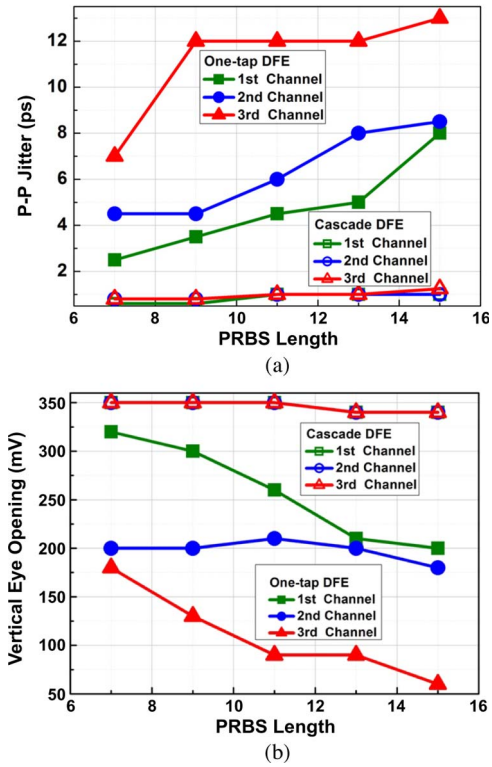

Fig. 9. (a) Simulated peak-to-peak jitter and (b) vertical eye opening versus the PRBS lengths.

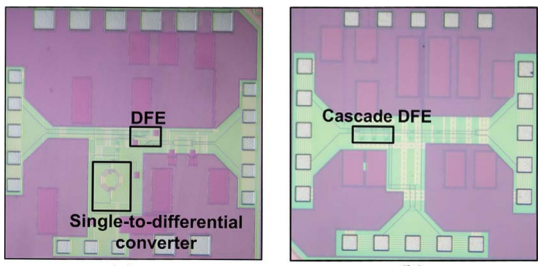

Fig. 10. Die photo for (a) a merged adder/DFF DFE and (b) a cascaded DFE.

DFEs for three different channels. The losses for the first, second, and third channels at 15 GHz are 10, 12, and 15 dB, respectively. The simulated peak-to-peak jitters of a one-tap DFE for three channels are 2.5, 4.5, and 7 ps, respectively. To cascade three one-tap DFEs, the simulated peak-to-peak jitters are less than 1 ps. Fig. 8 shows the simulated vertical eye openings of the retimed data versus the number of the cascaded one-tap DFEs. For a one-tap DFE, the vertical eye openings for three channels are 320, 200, and 180 mV, respectively. To cascade three one-tap DFEs, the simulated vertical eye openings are larger than 340 mV.

For a CMOS current-mode logic (CML) latch, if the input is small, the output within the latching mode is expressed as [9]

$$V_{\text{out}}(t) = V_{\text{out},0} \exp\left[\frac{(g_{mC}R - 1)t}{2RC}\right] \tag{8}$$

where R and C are the loading resistance and capacitance of a CML latch, respectively; g_{mC} is the transconductance of a cross-coupled pair; and $V_{\text{out},0}$ is the initial voltage in the latching mode. For a one-tap DFE operated at 30 Gb/s with

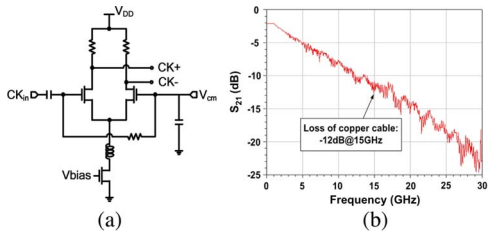

Fig. 11. (a) Single-to-differential converter. (b) Measured cable loss.

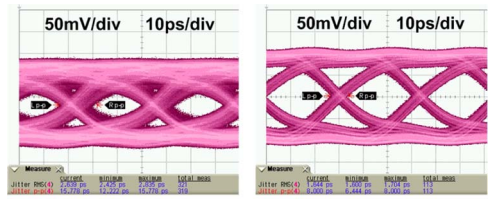

Fig. 12. Measured eye diagram for a 30-Gb/s PRBS of $2^7 - 1$ after (a) a one-tap DFE and (b) a cascaded DFE.

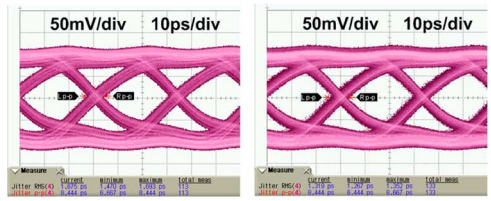

Fig. 13. Measured eye diagrams for a 30-Gb/s PRBS of (a) $2^{11} - 1$ and (b) $2^{15} - 1$ after a cascaded DFE.

channel loss of 15 dB, a CML DFF is composed of two CML latches. Assume $R = 130\ \Omega$, $I_1 = 2.7$ mA, $C = 20$ fF, $g_{mC} = 8$ mA/V, and the initial voltage is 110 mV. Since a CML DFF is composed of two latches, the calculated output swing of a one-tap DFE is 179 mV. Since the output swing of a one-tap DFE at 30 Gb/s is 179 mV, we can say that the one-tap DFE is a "soft decision" not a "hard decision." Similarly, the calculated output swing of the second stage of a cascaded DFE is 286 mV. Then, the output swing of the third stage of a cascaded DFE will be a "hard decision." The above results can be found in Fig. 8.

Figs. 7 and 8 reveal that the jitter and vertical eye opening of the retimed data are improved by cascading one-tap DFEs. However, the more one-tap DFEs are cascaded, the more power consumption is needed. Figs. 7 and 8 suggest that three cascaded DFEs are enough for the channel loss below 15 dB. For this reason, a cascaded DFE using three one-tap DFEs is chosen in this brief. Fig. 9(a) and (b) shows the simulated results of the peak-to-peak jitter and vertical eye opening, respectively, for a one-tap DFE and a cascaded DFE versus the different PRBS lengths at 30 Gb/s. From Fig. 9(a), for a one-tap DFE under a channel loss of 15 dB and a PRBS of $2^{15} - 1$, the peak-to-peak jitters and vertical eye openings of the retimed data are higher than 12 ps_{pp} and lower than 75 mV, respectively. For a cascaded DFE under the same conditions, its peak-to-peak jitters and vertical eye openings of the retimed data are below 2 ps_{pp} and higher than 340 mV, respectively. According to the simulation results in Fig. 9(b), a cascaded DFE can suppress the ISI under different channel losses and PRBS lengths to achieve a good vertical eye opening and jitter for the retimed data.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	[1]	[2]	[5]	[6]	A one-tap DFE	A cascade DFE
CMOS	90nm	90nm	90nm	65nm	65nm	65nm
Data Rate	7Gb/s (Half Rate)	6Gb/s (Quarter Rate)	19Gb/s (Half Rate)	40Gb/s (Full Rate)	30Gb/s (Full Rate)	30Gb/s (Full Rate)
Inductor	No	No	No	Yes	No	No
Architecture	Current integrate	Soft decision	Threshold adjust latch	Back-gate Feedback (Separate adder/DFF)	Back-gate Feedback (Merged adder/DFF)	Back-gate Feedback (Merged adder/DFF)
Tap Number	2	2	1	1	1	1
Channel loss (dB)	15	6.2	11	15	12	12
Retimed Data jitter (ps)	N/A	N/A	N/A	13.1	15.8	8
Supply (V)	1	1	1	1.2	1	1
Power (mW)	9.3	5	38	45	27	55
Area (um^2)	65×85	45×98	155×122	180×340	60×80	120×55

III. EXPERIMENTAL RESULTS

Fig. 10(a) shows the die photo of the one-tap DFE, and its core area is 0.06 mm × 0.08 mm. Fig. 10(b) shows the die photo of a cascaded DFE, and its core area is 0.12 mm × 0.055 mm. Since the pattern generator (Anritsu 1803A) only provides a single-ended clock, a single-to-differential converter is needed to generate the differential clocks for a DFE circuit. Fig. 11(a) shows the single-to-differential converter for the one-tap DFE. To reduce the output swing mismatch of the single-to-differential converter, a shunt inductor is adopted, which has an area of $80 \times 130\ \mu m^2$. With this inductor, the output swing mismatch of the single-to-differential converter is reduced from 19% to 6%. For the cascaded DFE, off-chip differential clocks are provided. Fig. 11(b) shows the measured S_{21} parameter of a coaxial cable. The cable loss is -12 dB at 15 GHz. When a one-tap DFE receives the data with a PRBS of $2^7 - 1$ from the above coaxial cable, the measured output eye diagram is shown in Fig. 12(a). The eye diagram has a vertical eye opening of 50 mV. The peak-to-peak jitter is 16 ps, and the rms jitter is 2.84 ps.

Fig. 12(b) shows the measured output eye diagram when a cascaded DFE receives the same data from the above coaxial cable. The eye diagram has a vertical eye opening of 100 mV. The peak-to-peak jitter is 8 ps, and the rms jitter is 1.7 ps. When a one-tap DFE receives the data with the PRBSs of $2^{11} - 1$ and $2^{15} - 1$ from the above coaxial cable, the eye diagrams are closed. On the other hand, when a cascaded DFE receives the data with the PRBSs of $2^{11} - 1$ and $2^{15} - 1$ from the above coaxial cable, the measured output eye diagrams are shown in Fig. 13(a) and (b), respectively. The experimental results show that the cascaded DFE compensates the channel loss and suppresses the ISI caused by different PRBS lengths. The measured bit error rate is below 10^{-11} for a one-tap DFE with a PRBS of $2^7 - 1$. The measured bit error rates are below 10^{-12} for a cascaded DFE with the PRBSs of $2^7 - 1$, $2^{11} - 1$, and $2^{15} - 1$. The power dissipation values of the one-tap DFE and a cascaded DFE are 27 and 55 mW, respectively, from a supply of 1 V without buffers. The performance summary and comparison with previous works are summarized in Table I.

In [6], the DFE with inductors operates at 40 Gb/s. It consumes 45 mW for a 1.2-V supply, and the chip area is $180 \times 340\ \mu m^2$. Owing to the merged adder/DFF, the power consumption of the proposed one-tap DFE at 30 Gb/s is 27 mW with a 1-V supply. The chip area of the one-tap DFE is $60 \times 80\ \mu m^2$. The area of the proposed DFE is only 8% of that in [6].

IV. CONCLUSION

In this brief, a one-tap DFE using a merged adder/DFF by the back-gate feedback technique has been presented. Owing to this merged adder/DFF, the delay time and power of a one-tap DFE are improved. The experimental results show that this one-tap DFE achieves the operation speed of 30 Gb/s without passive inductors. Furthermore, a cascaded DFE using three one-tap DFEs has been also presented. According to the experimental results, this cascaded DFE improves by about 49% peak-to-peak jitter and 100% vertical eye opening than a one-tap DFE without any speed penalty. However, the power of a cascaded DFE is increased to 55 mW.

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